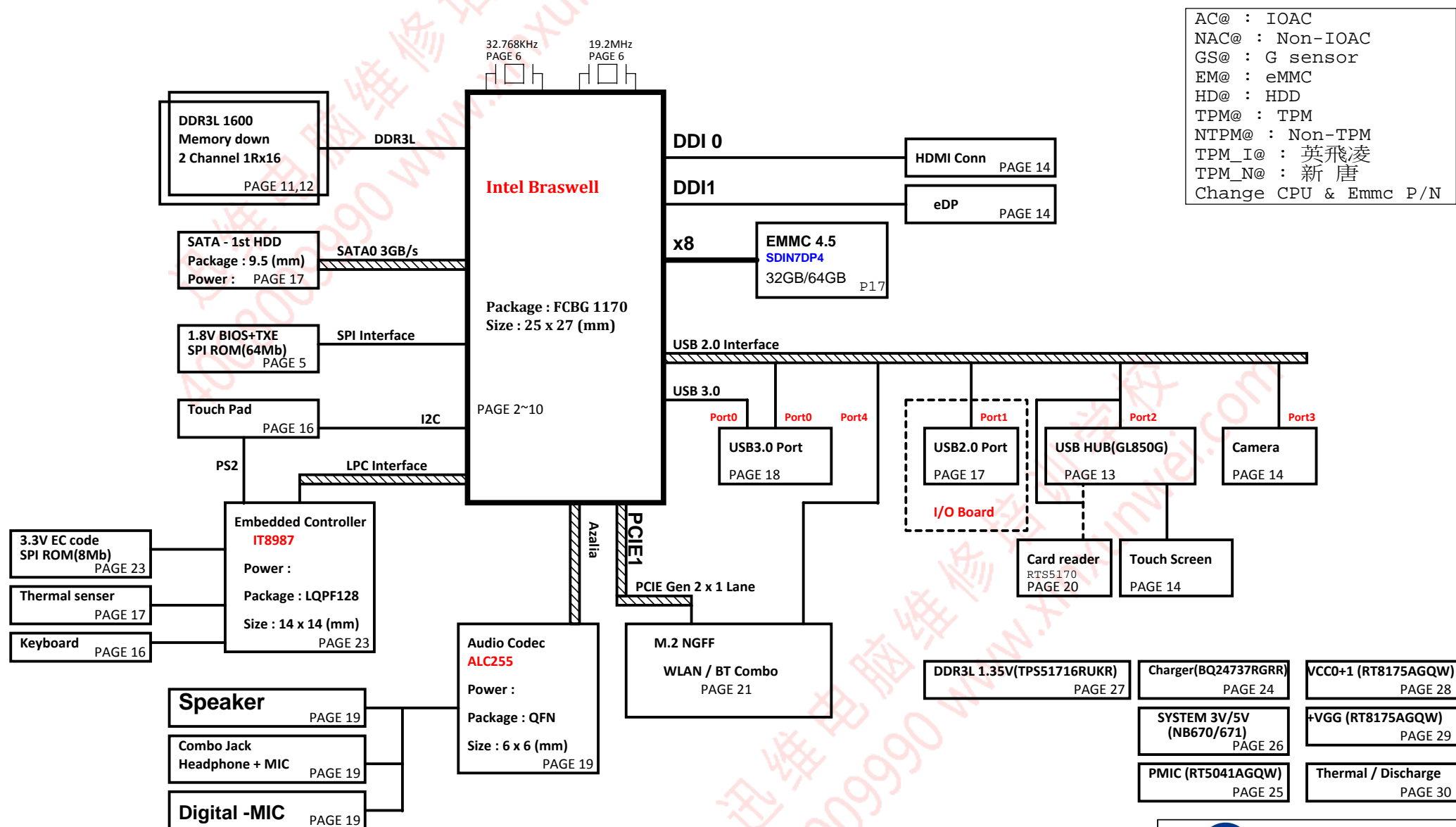
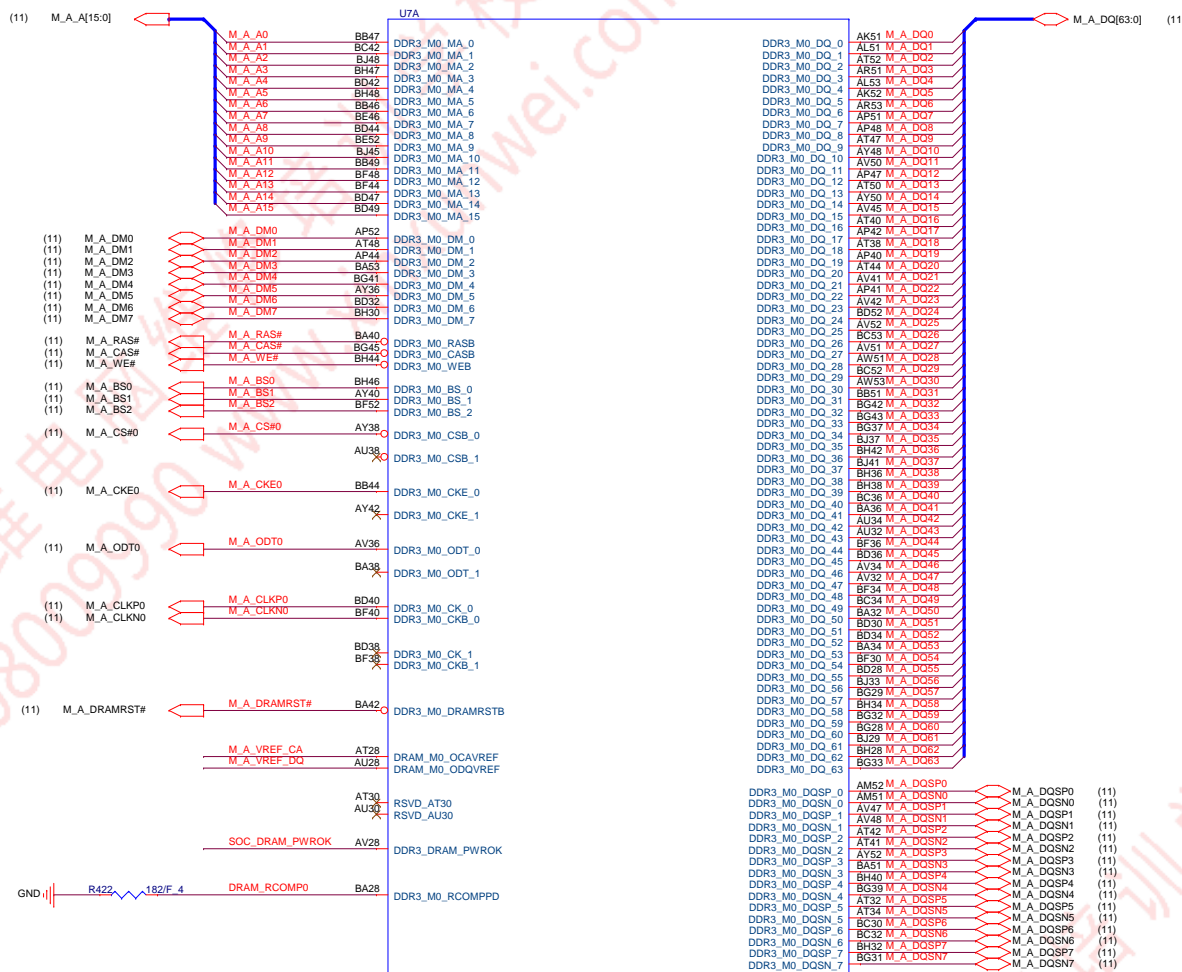


ZHX_ZHXS UMA(11.6")

Intel Braswell Platform Block Diagram



+1.35VSUS (3,9,11,12,22,27)
+3V_S5 (3,5,9,13,15,16,18,23,25)

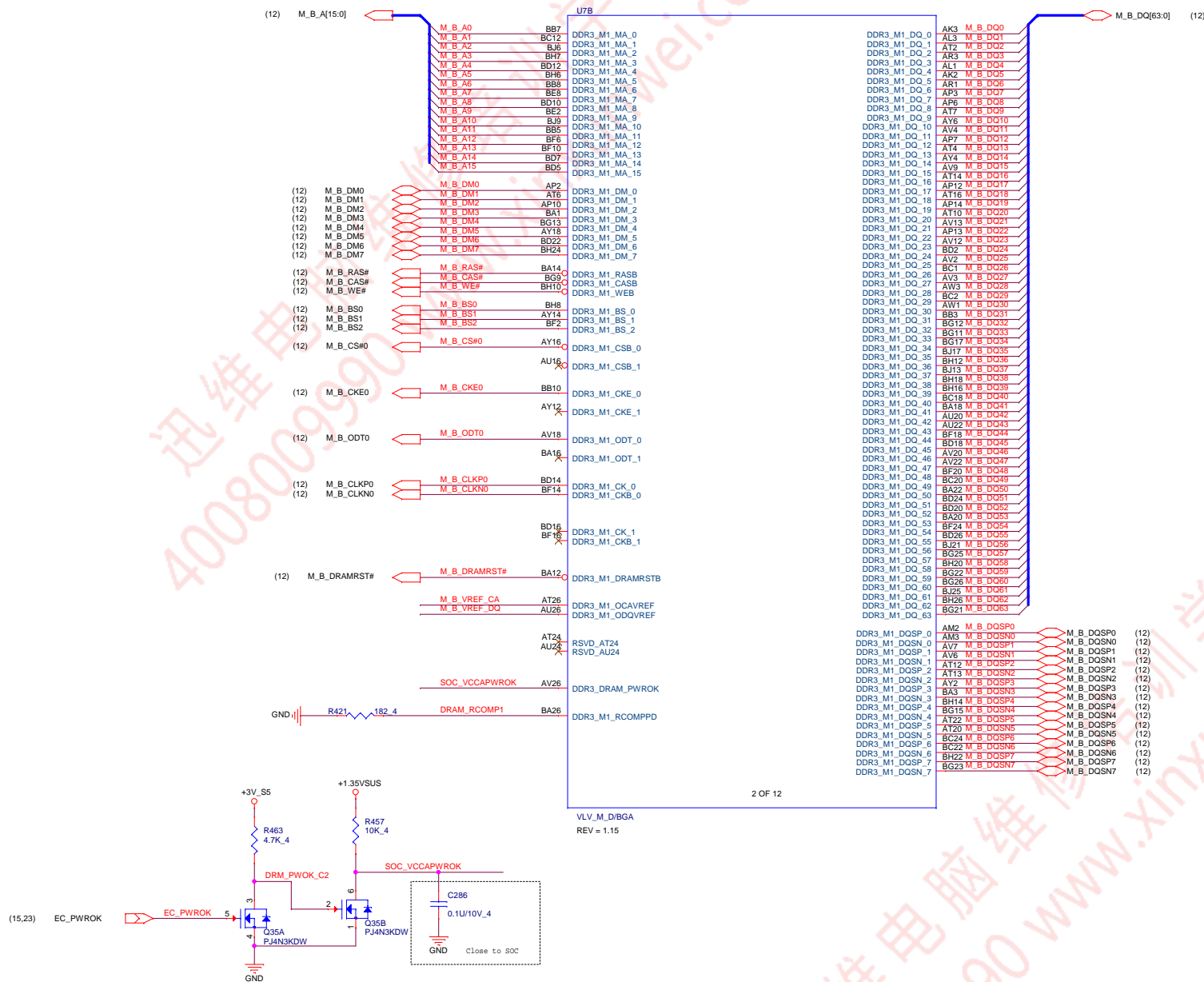


Channel 0	Channel 1	SOC Supported Memory Operation Speed
1333 MHz	X	1066 MHz
1600 MHz	X	1600 MHz
1333 MHz	1333 MHz	1066 MHz
1600 MHz	1600 MHz	1600 MHz

Channel 0 need to
be populated first for the platform to power on

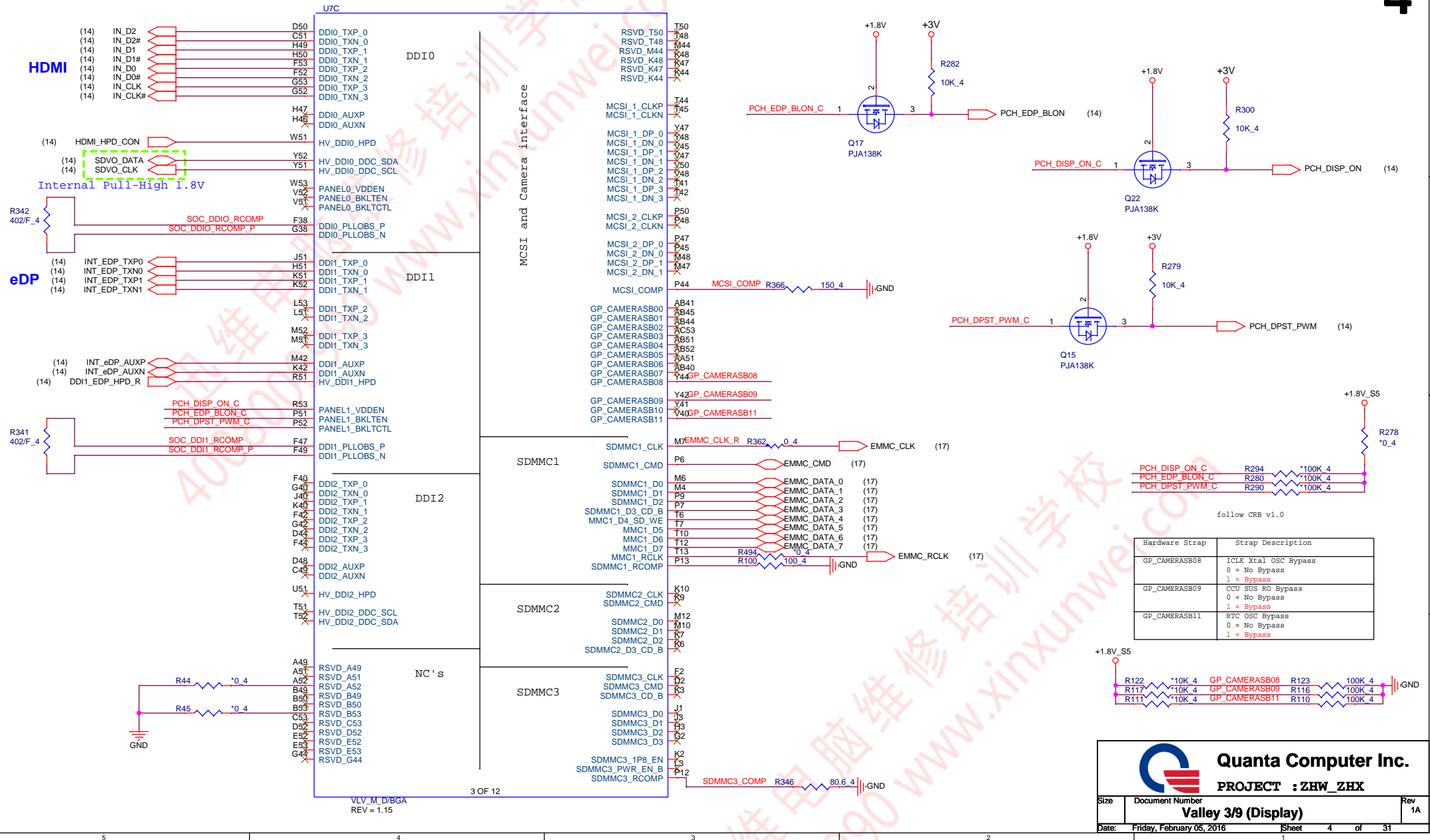
Quanta Computer Inc.
PROJECT : ZHW_ZHX

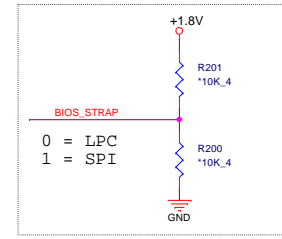
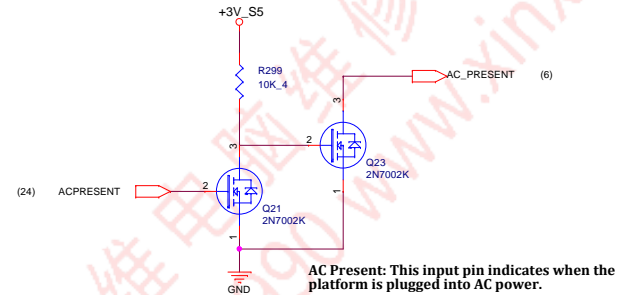
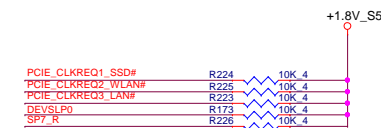
Size	Document Number	Rev
	Valley 1/9 (DDRA)	1A
Date:	Friday, February 05, 2016	Sheet 2 of 31

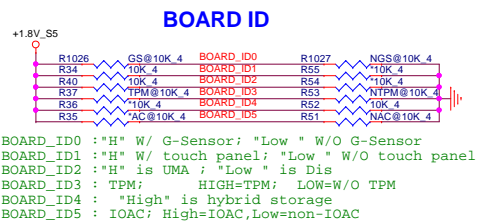
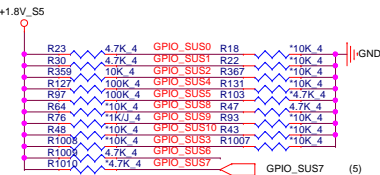


(7,9,13,14,15,16,17,18,19,20,21,22,23,26,27,28,29,30)

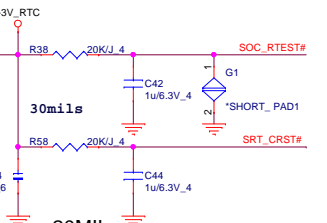
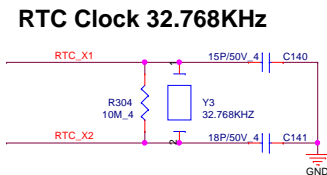
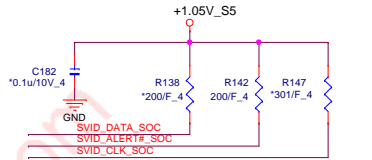
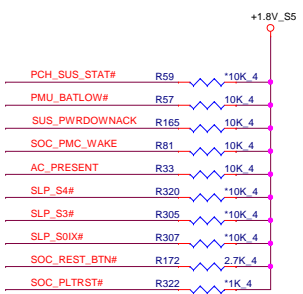
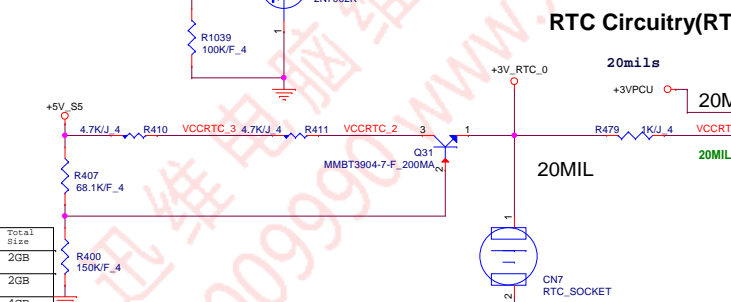
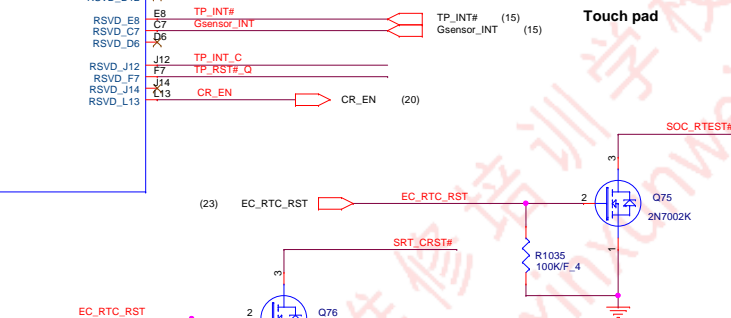
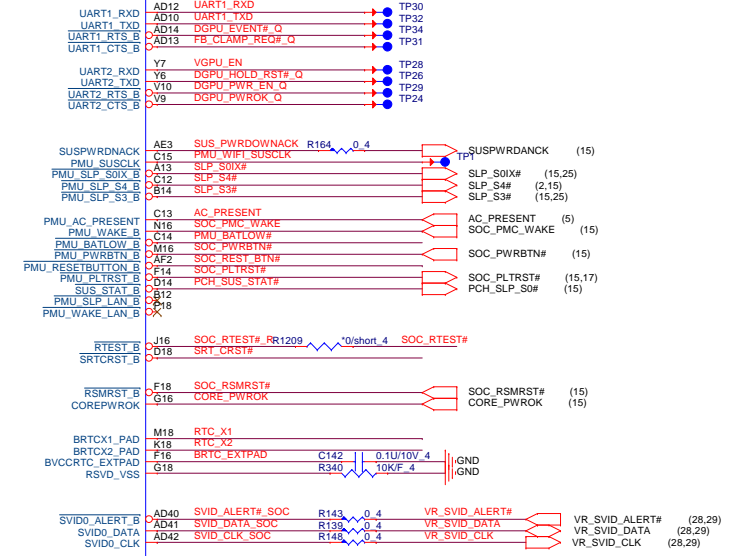
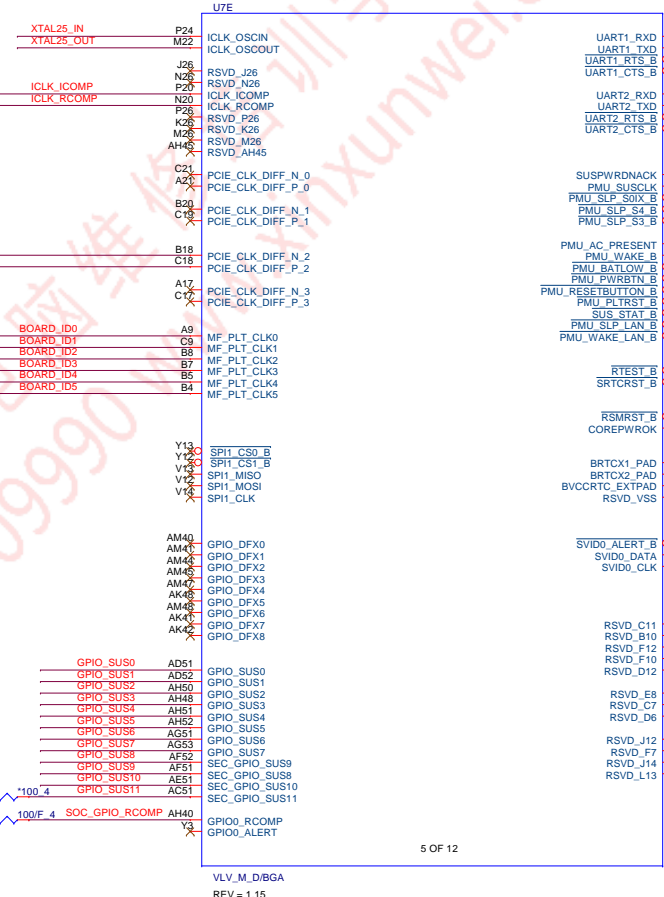
+3V

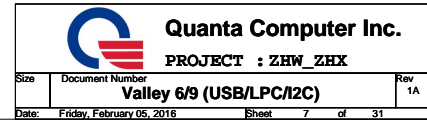


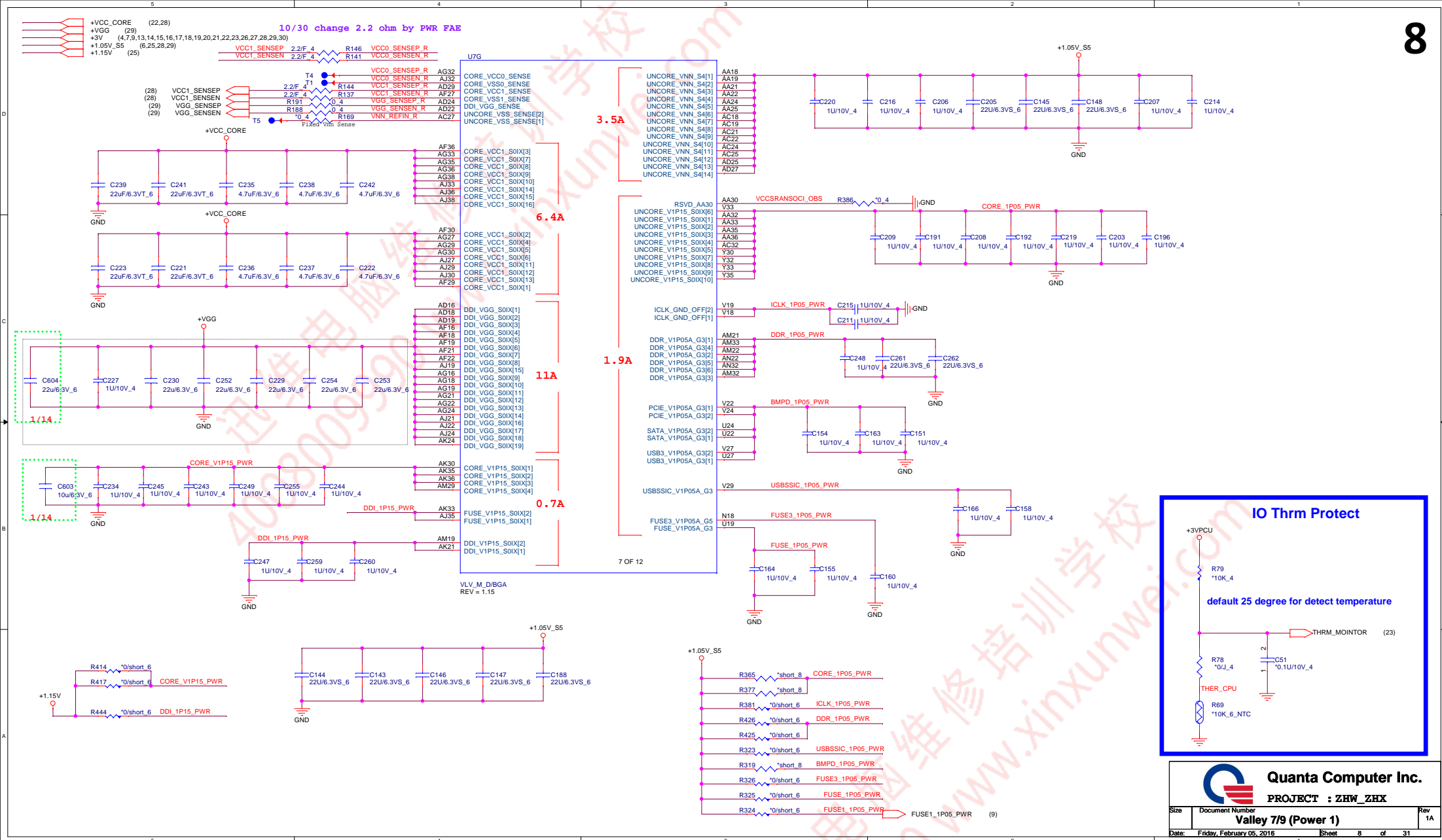


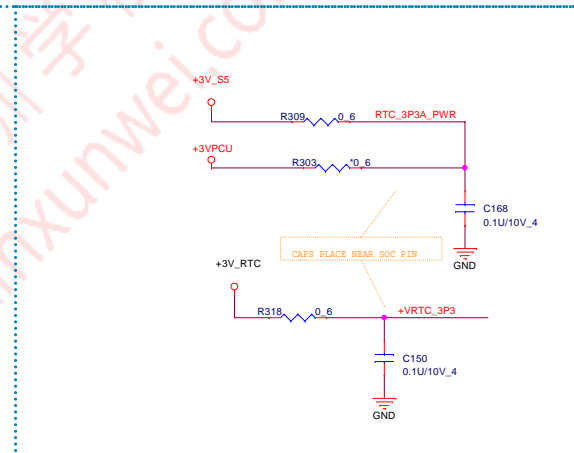
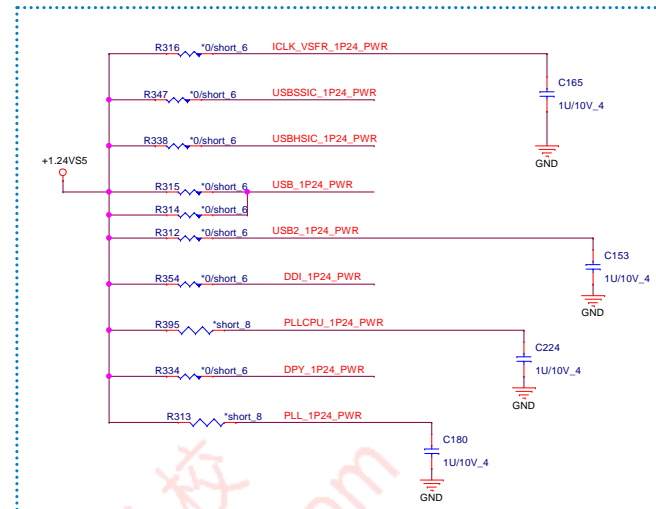


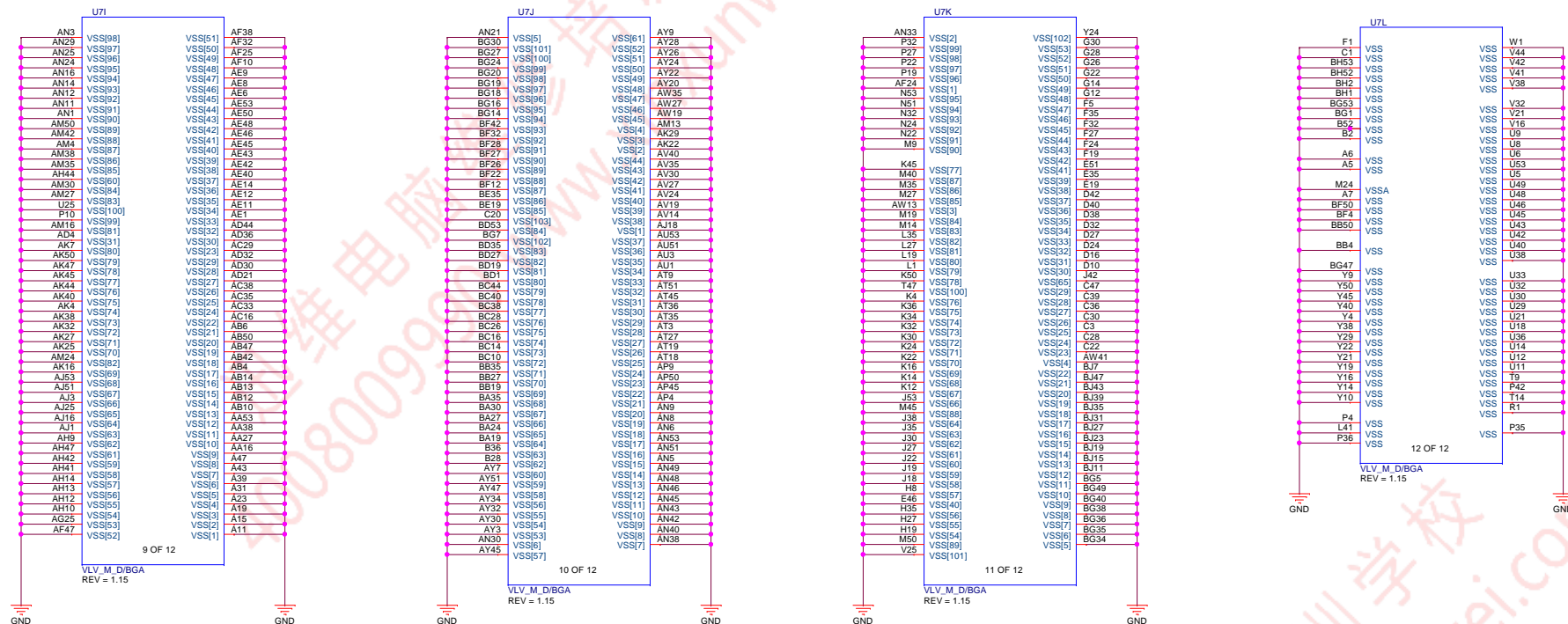
Vendor	RAM_ID	PN	Mfr. PN	Freq.	Size	Total Size
Hynix	0000	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHz	4Gb	2GB
Samsung	0001	AKD5JG0T504	K4B4G1646E-BYK0	1600MHz	4Gb	2GB
Hynix	0010	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHz	4Gb	4GB
Samsung	0011	AKD5JG0T504	K4B4G1646E-BYK0	1600MHz	4Gb	4GB
	1234					











DDR3L MEMORY CHANNEL A

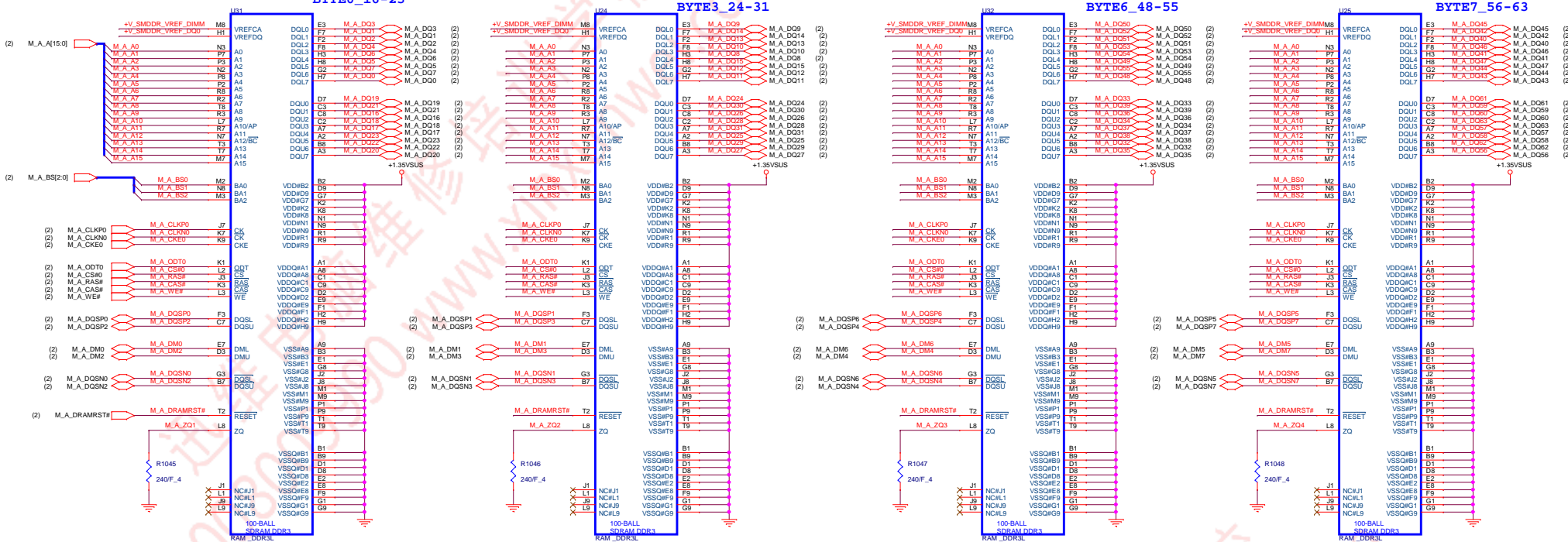
BYTE0_0-7
BYTE0_16-23

BYTE0_8-15
BYTE3_24-31

BYTE4_32-39
BYTE6_48-55

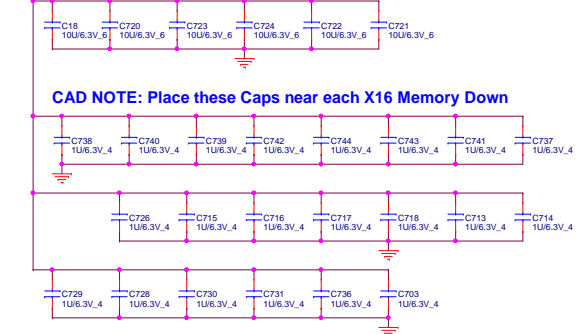
BYTE5_40-47
BYTE7_56-63

11



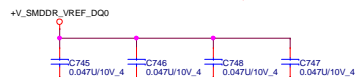
DE-CAPS FOR MEMORY CHANNEL A

CAD note: Distributed around all DRAM devices (CHA)

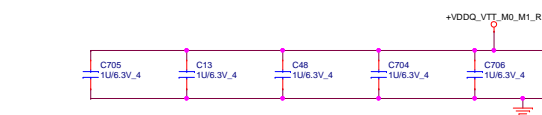


CAD NOTE: Place these Caps near each X16 Memory Down

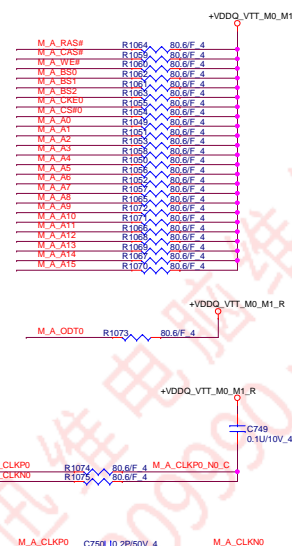
PLACE 2 CAPS NEAR EACH DDR3L IC



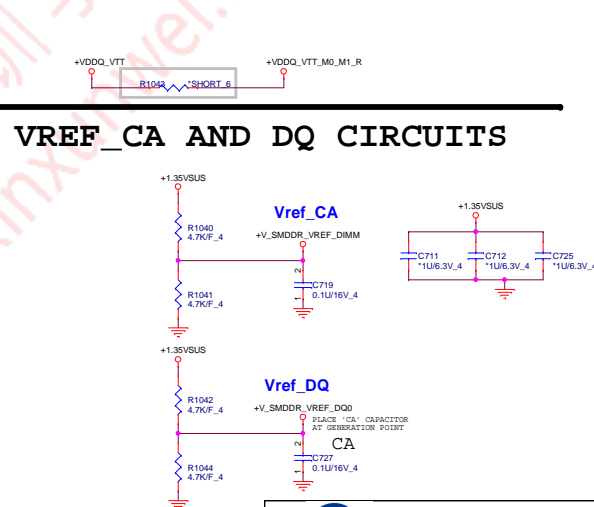
Place these Caps near Memory Down CA & DQ pin

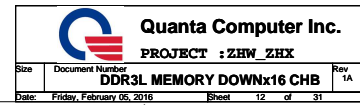


VTT TERMINATIONS

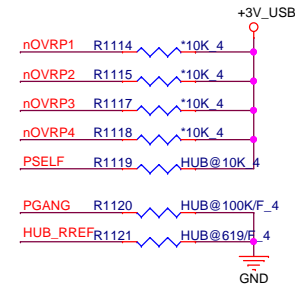


VOLTAGE MERGE





13



close each other

USB(IN)

USBP2-
USBP2+

Touch Panel

TS_USB-
TS_USB+

USBP2-
USBP2+

USBP2 CAR N
USBP2 CAR P
HUB@0_4
USB HUB N1
USB HUB P2

GL850G-OHY50

20130619 Follow vendor's suggestion(Close to pin 21)

52.4mA

TP49

TP48

USB_HUB 5V

3V_USB

RESET#_USB

USB_CR_P

USB_CR_N

USBP2 CAR N

USBP2 CAR P

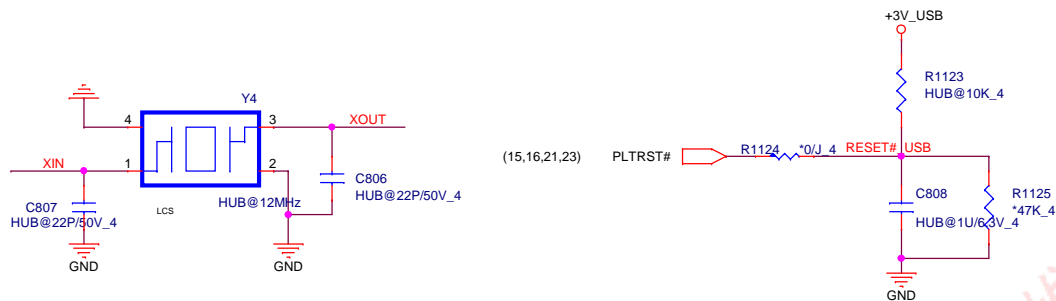
NTS@0_4

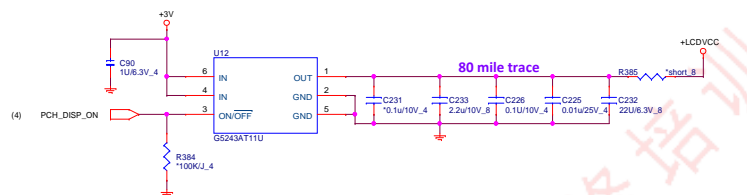
HUB@0_4

HUB@GL850G-OHY50

close each other

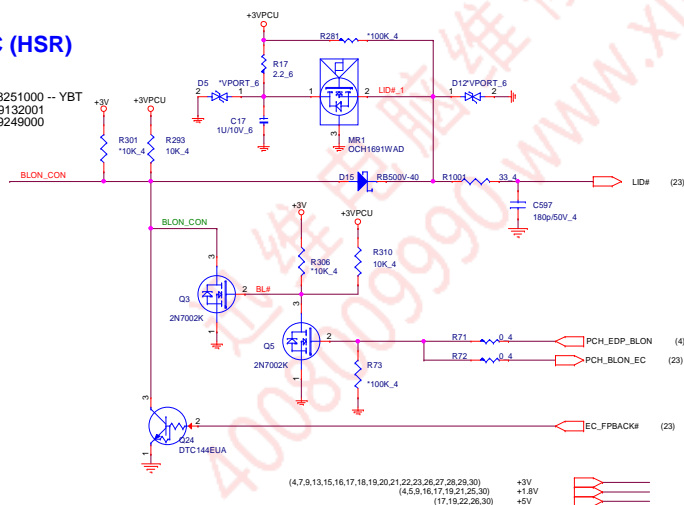
OVCURN#
Floating
Pull high



LVDS Conn.

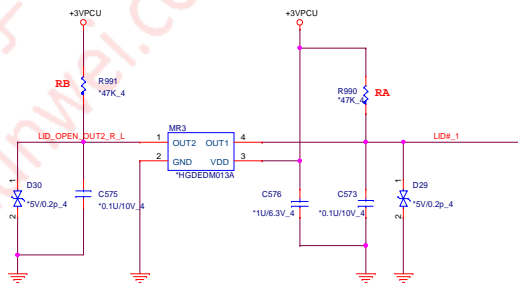
HALL IC (HSR)

1st source : EOD
2nd source : AL008251000 -- YBT
3rd source : AL009132001
4th source : AL009249000

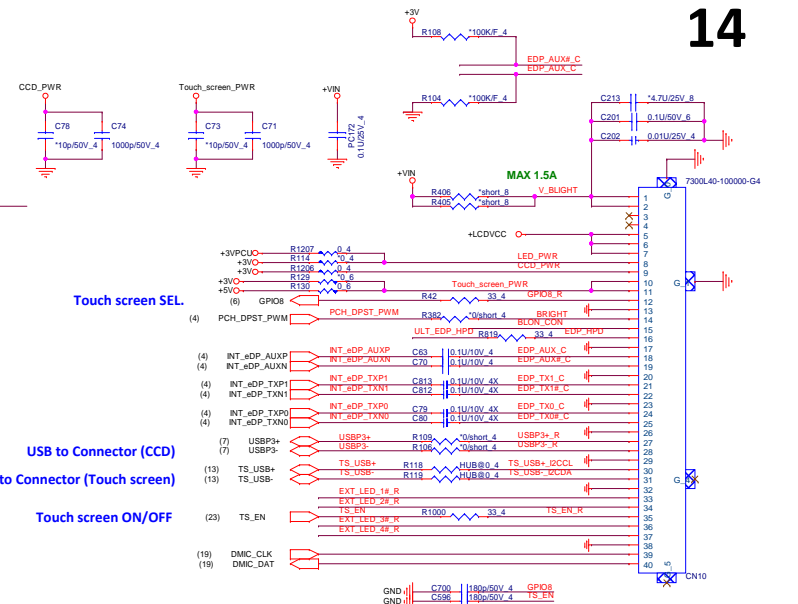


GMR Sensor

RA/RB can be unstuffed if using GMR



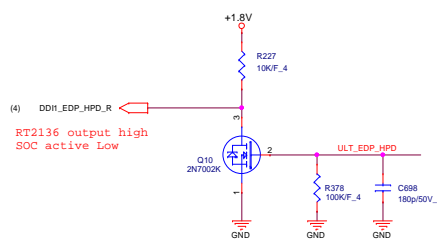
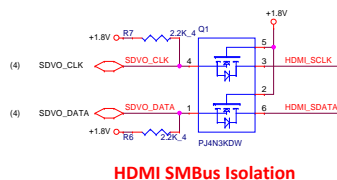
Touch screen SEL.



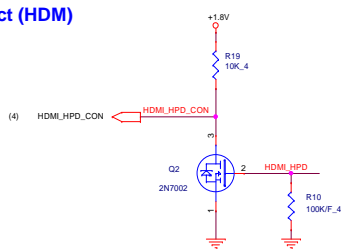
USB to Connector (CCD)

USB to Connector (Touch screen)

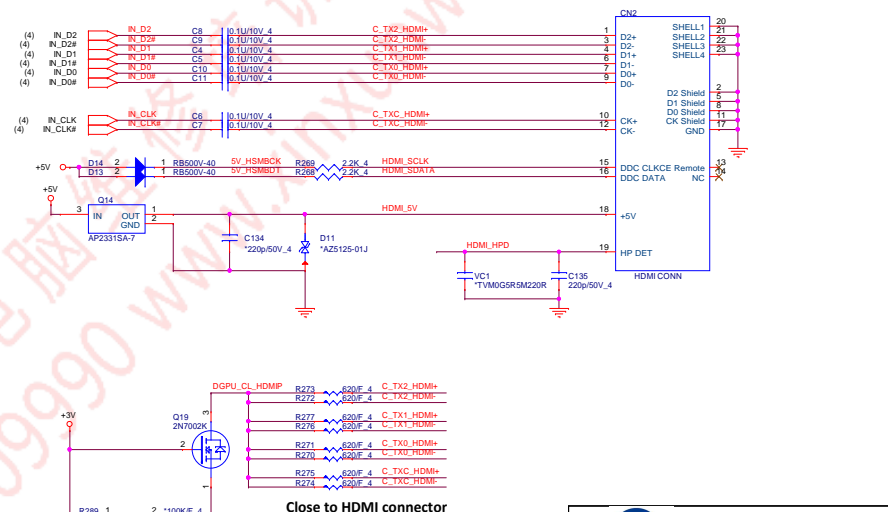
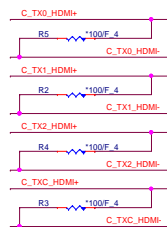
Touch screen ON/OFF

**HDMI Conn.**

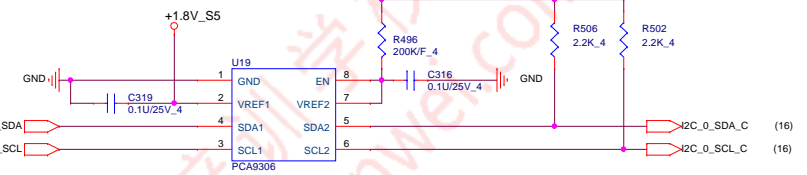
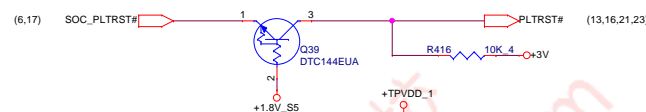
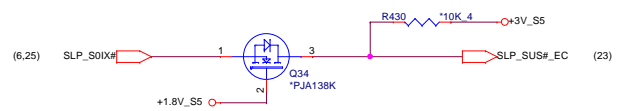
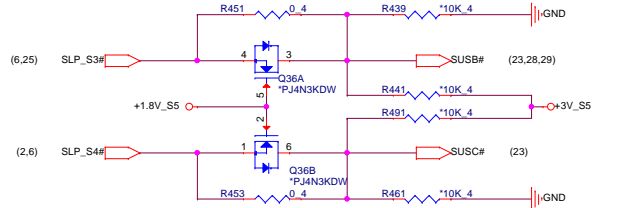
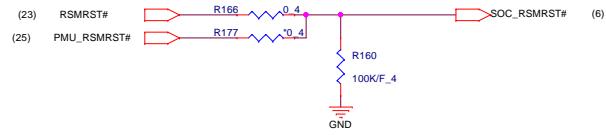
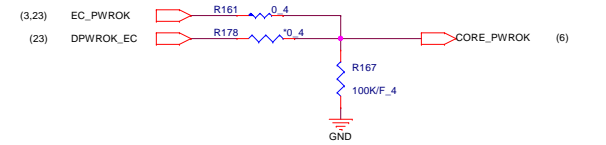
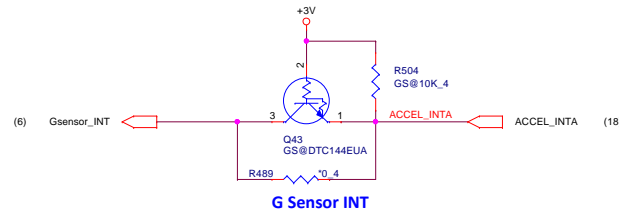
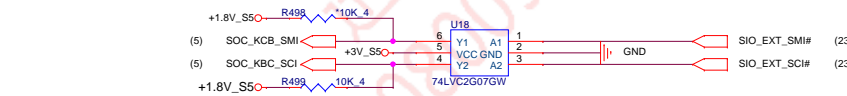
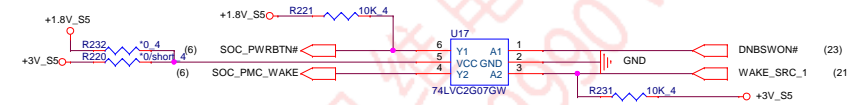
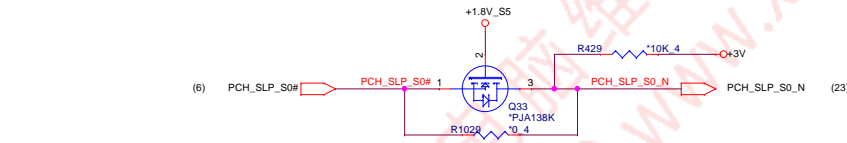
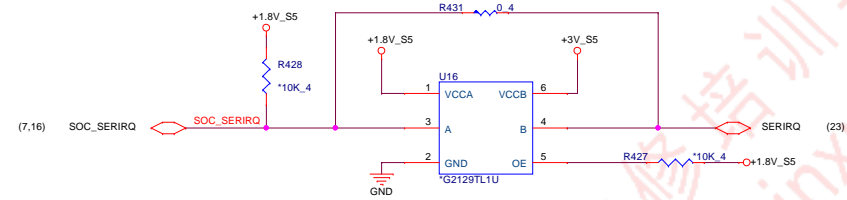
HDMI-detect (HDM)



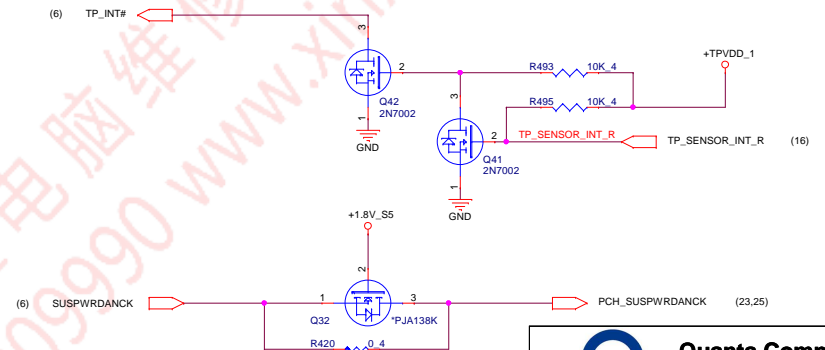
EMI (EMC)



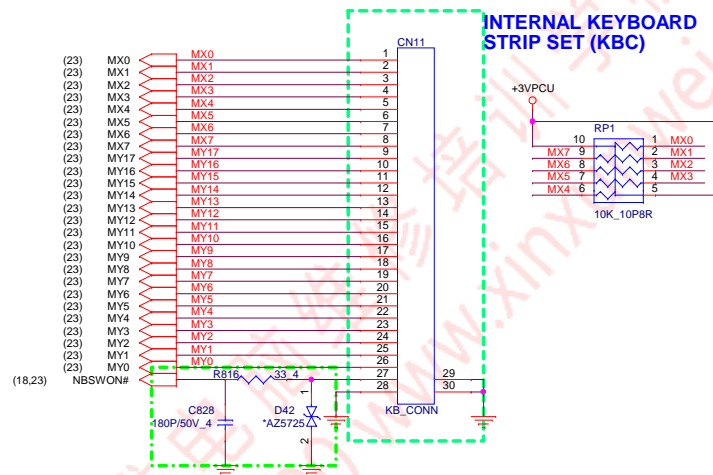
+1.8V_S5 (4,5,6,7,9,23,24,25,28,29)
 +3V_S5 (2,3,5,9,13,16,18,23,25)
 +1.8V (4,5,9,14,16,17,19,21,25,30)
 +3V (4,7,9,13,14,16,17,18,19,20,21,22,23,26,27,28,29,30)



For Touch pad : POWER-A

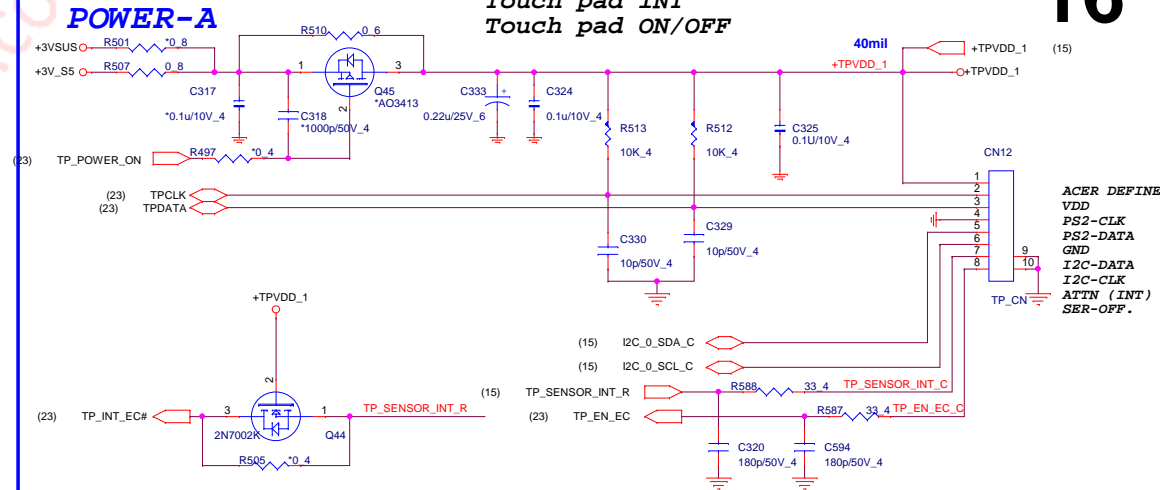


KEYBOARD (KBC)



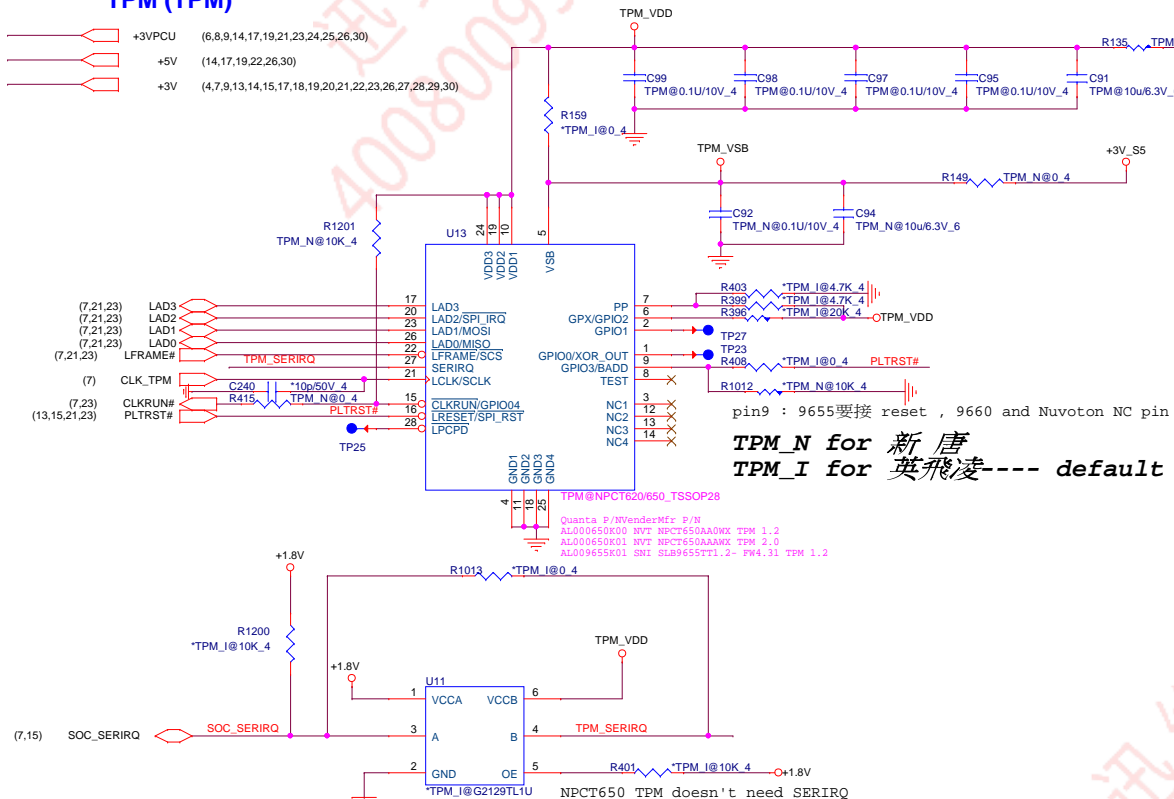
TOUCH PAD (TPD)

Touch pad I2C
Touch pad INT
Touch pad ON/OFF



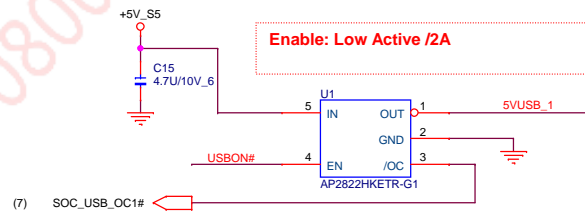
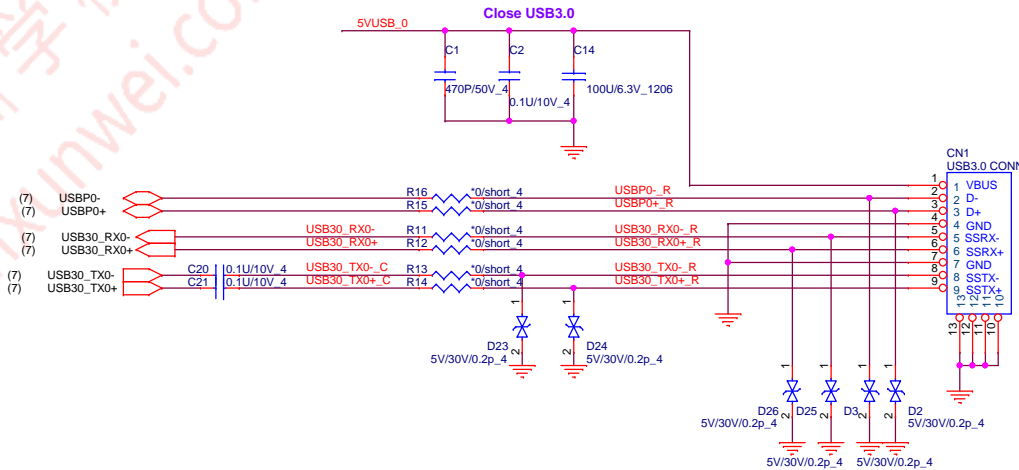
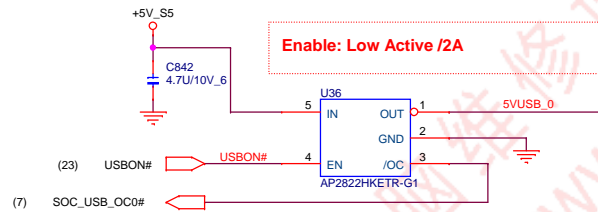
16

TPM (TPM)

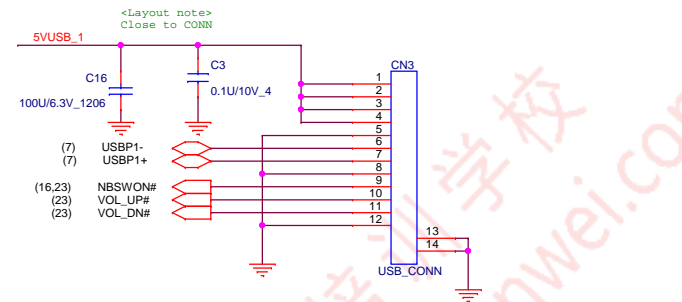


note: serie need to add level shift

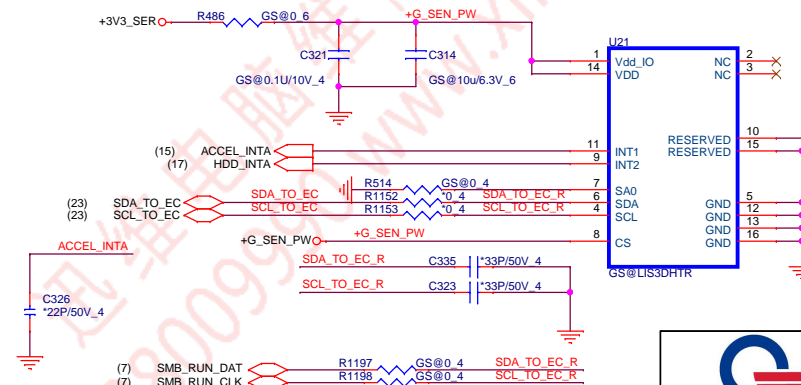
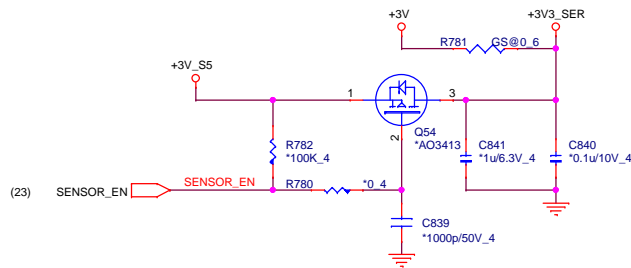
USB 3.0 Connector



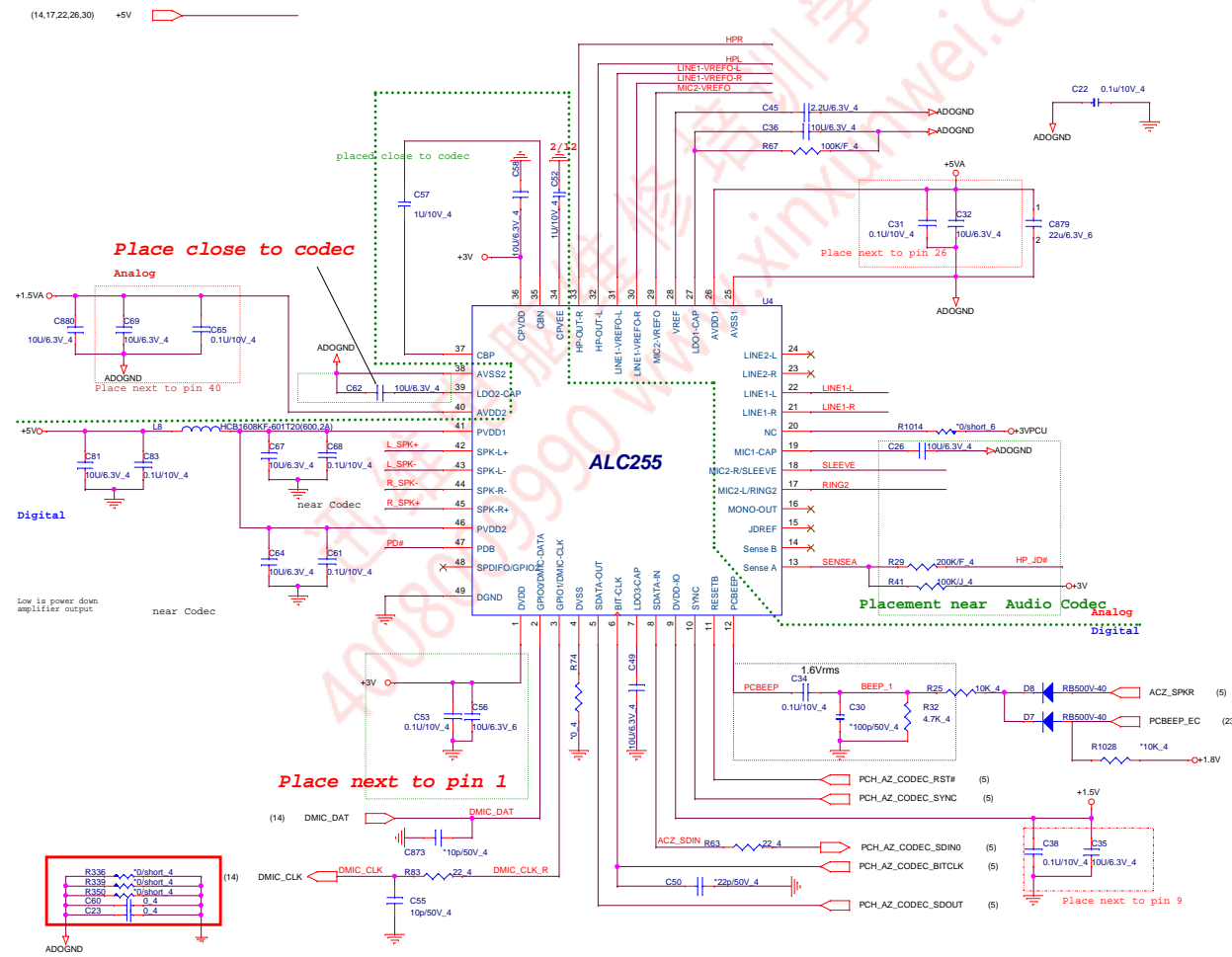
D/B Port USB 2.0



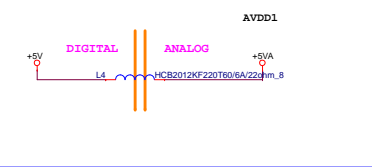
G-sensor



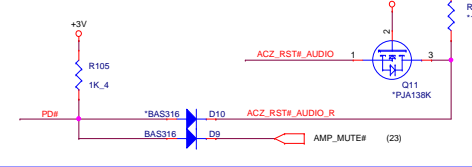
Codec(ADO)



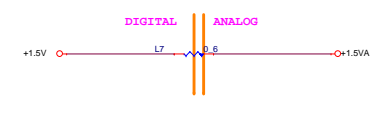
Codec PWR 5V(ADO)



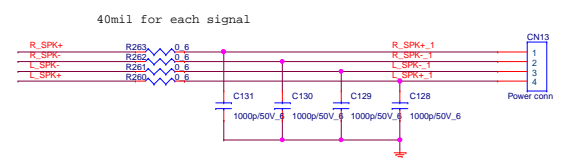
Mute(ADO)



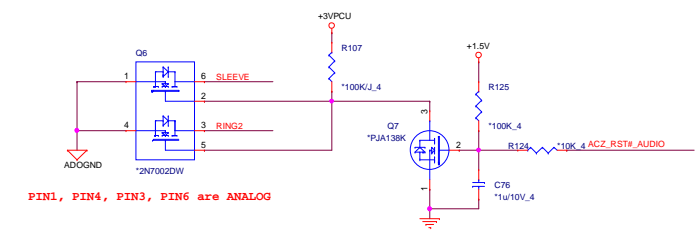
Codec PWR 1.5V(ADO)



Internal Speaker



Grounding circuit(ADO)



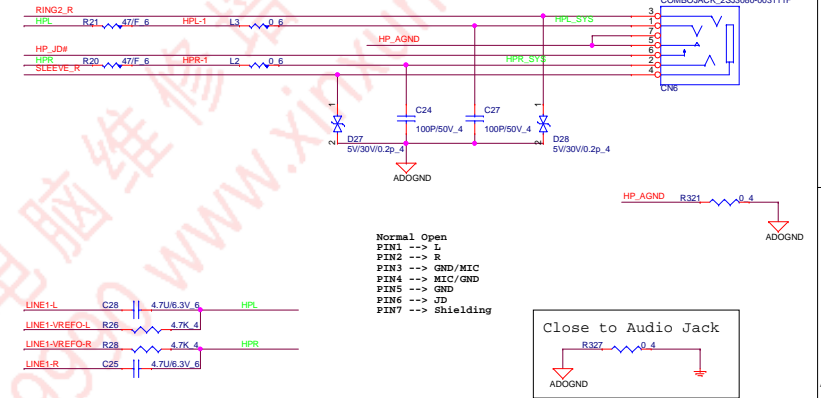
Microphone

move to LED BD

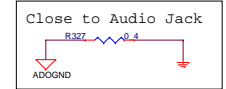


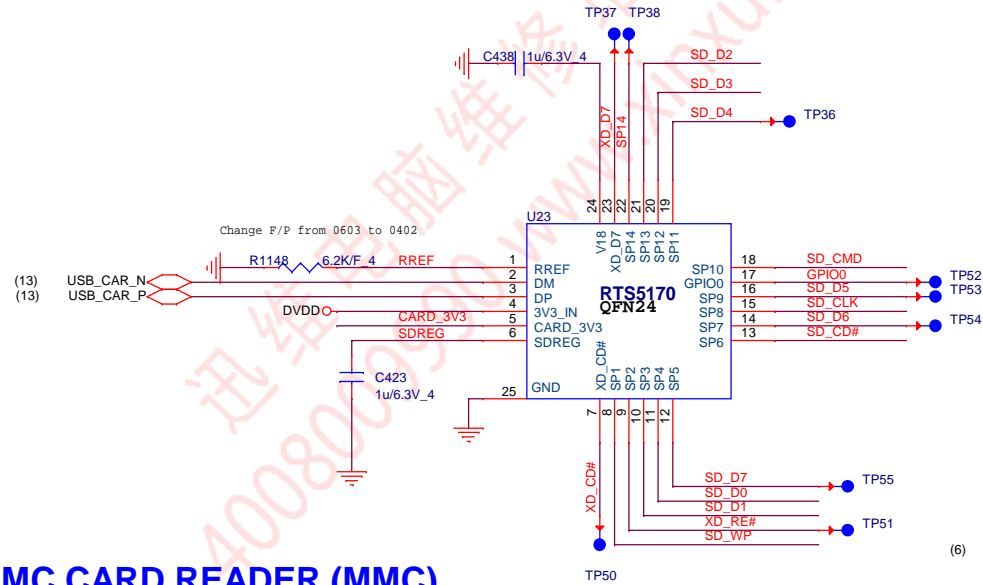
note : change next P/N: DFTJ06FR653
CONN DIP PHONE JACK 6P FR(H4.5)
foot print: phjk-2sj3072-108111f-6p

HP_MIC 上/下/左/右包覆AGND

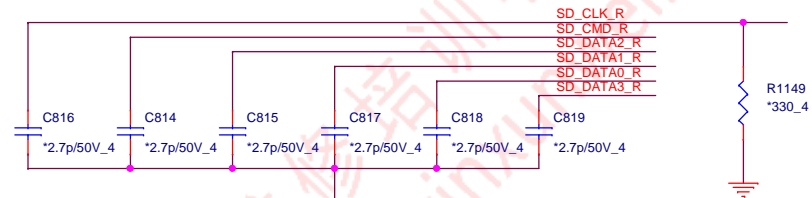
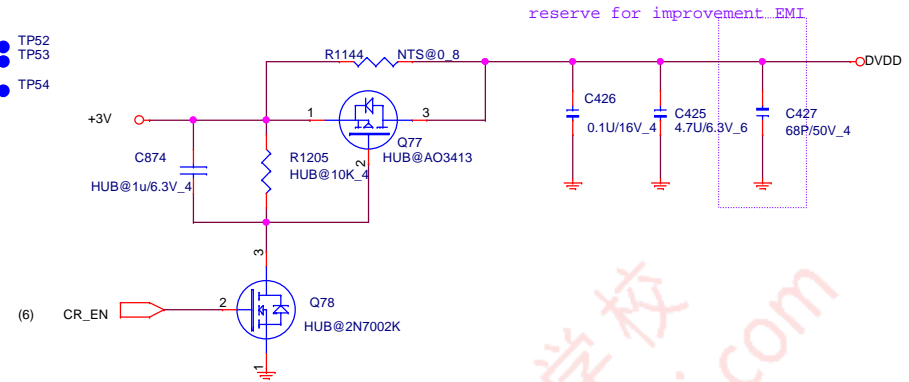
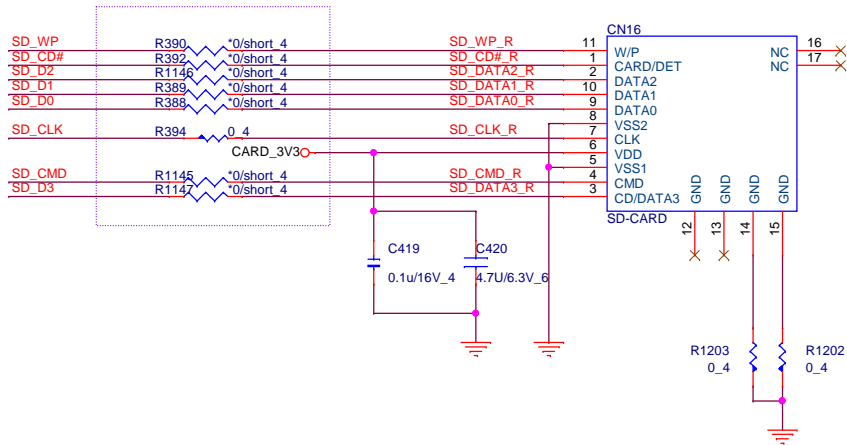


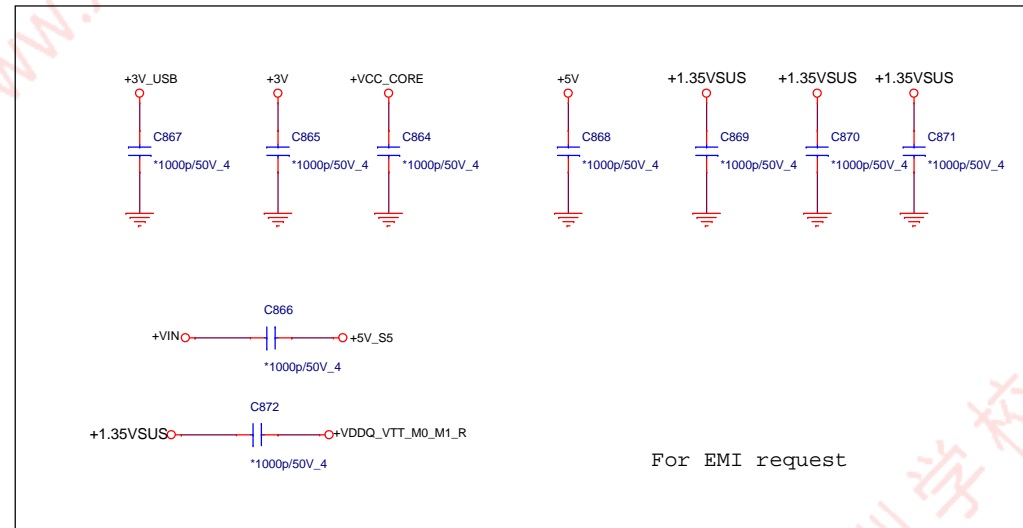
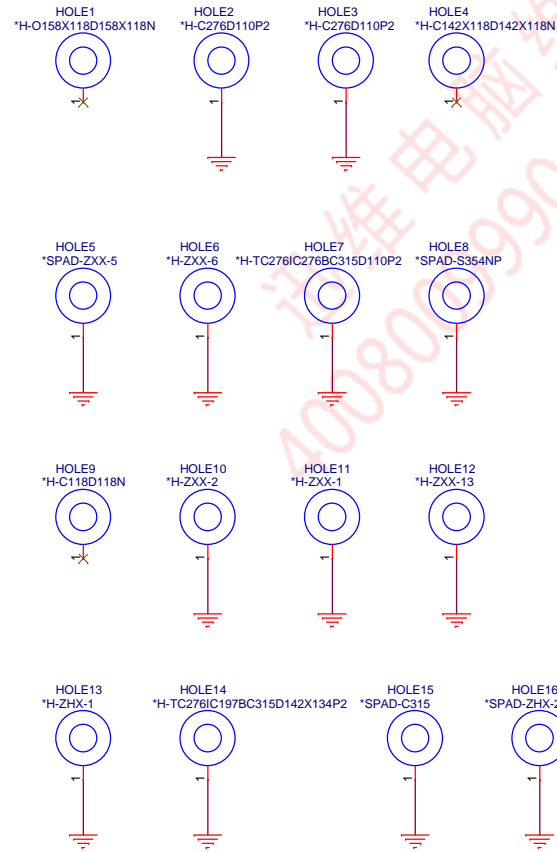
```
Normal Open
PIN1 --> L
PIN2 --> R
PIN3 --> GND/MIC
PIN4 --> MIC/GND
PIN5 --> GND
PIN6 --> JD
PIN7 --> Shielding
```



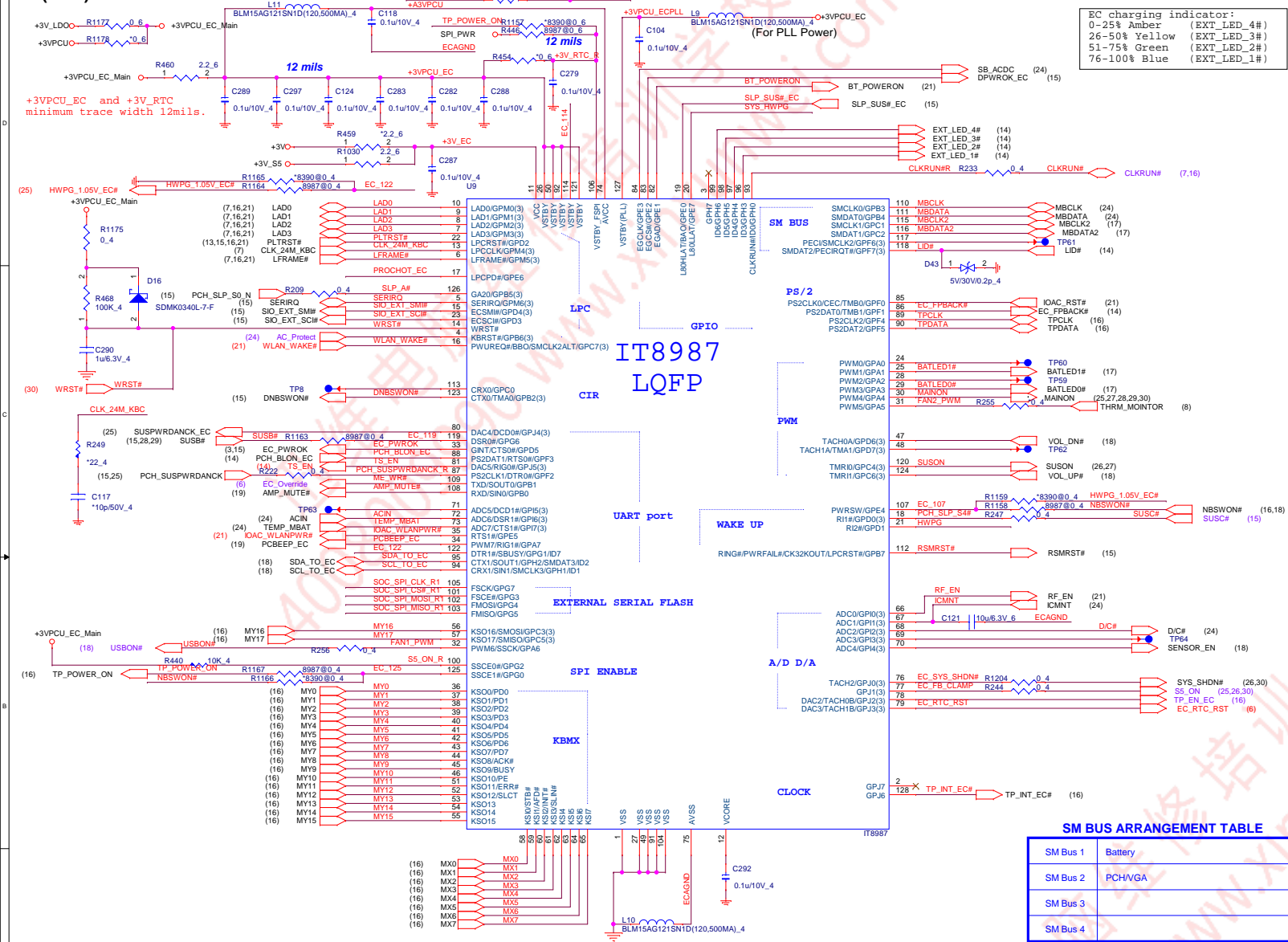


SD/MMC CARD READER (MMC)



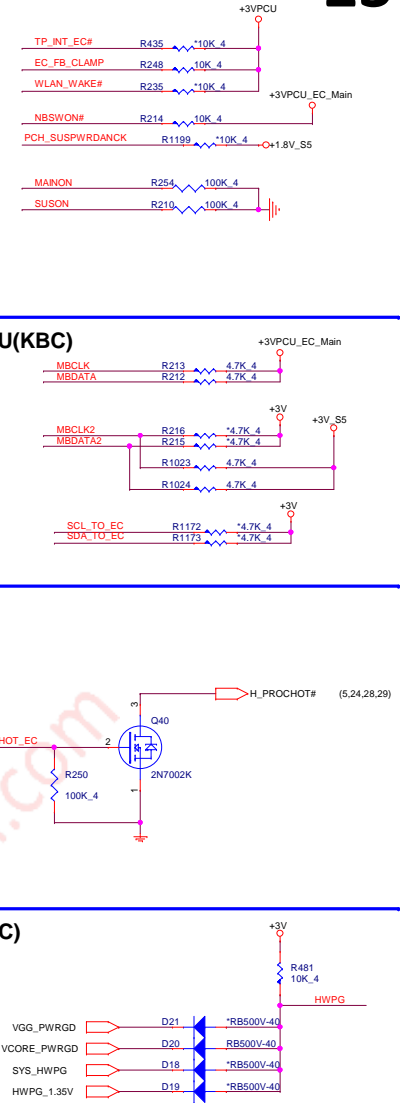


EC(KBC)

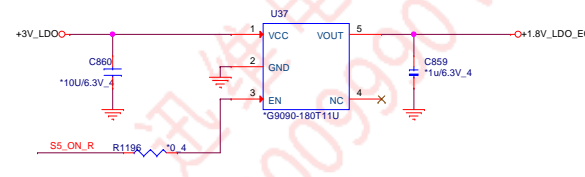
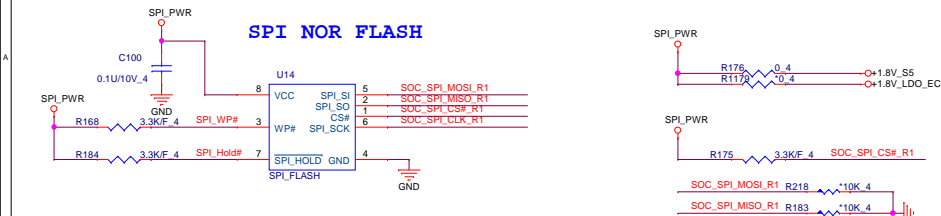


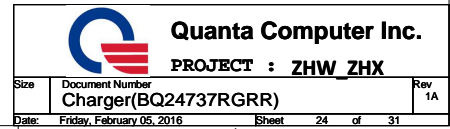
SM BUS PU(KBC)

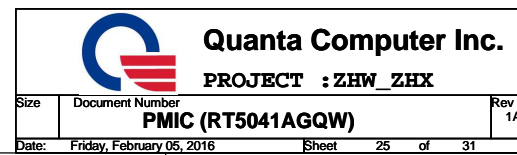
HWPG(KBC)

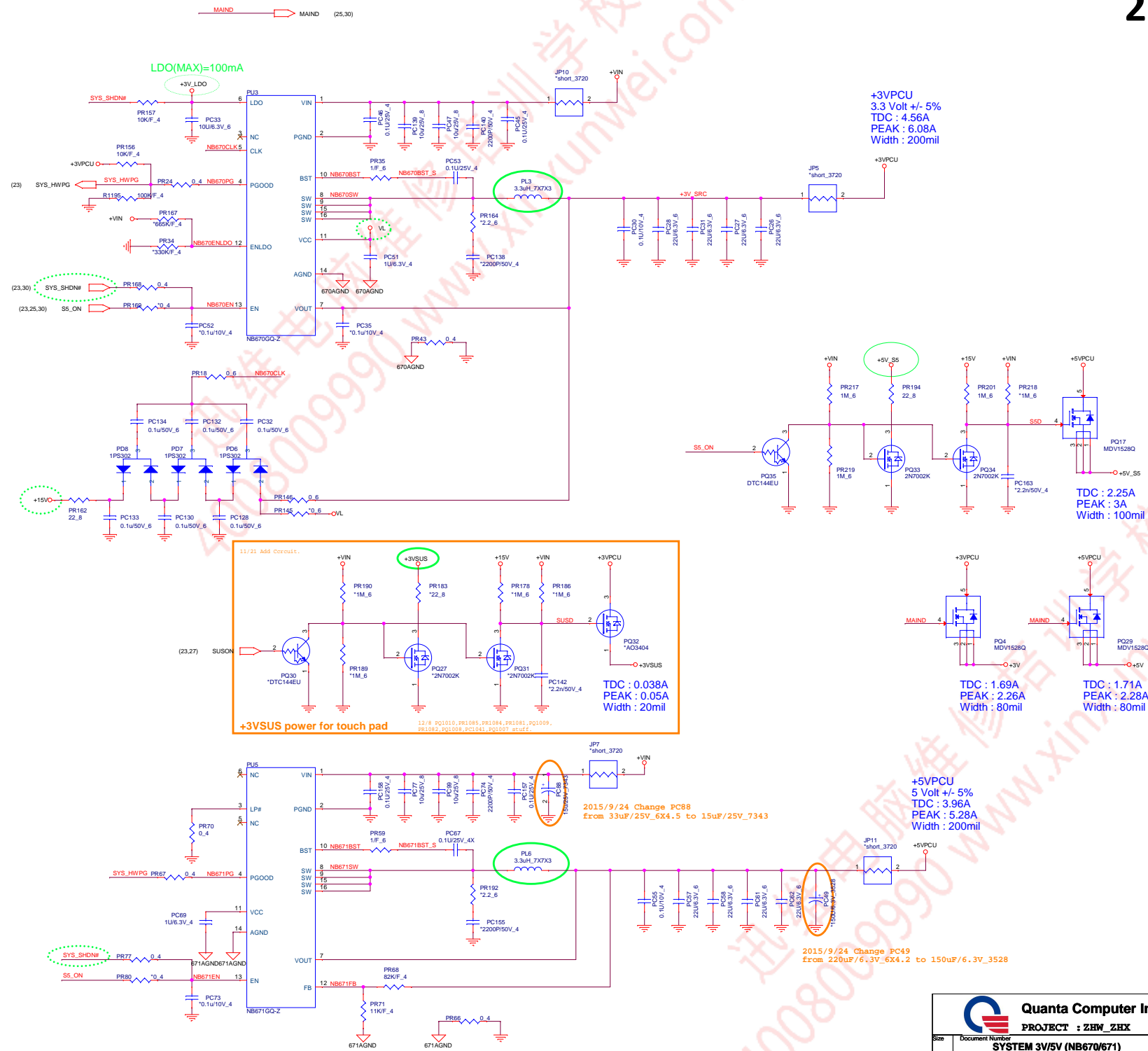


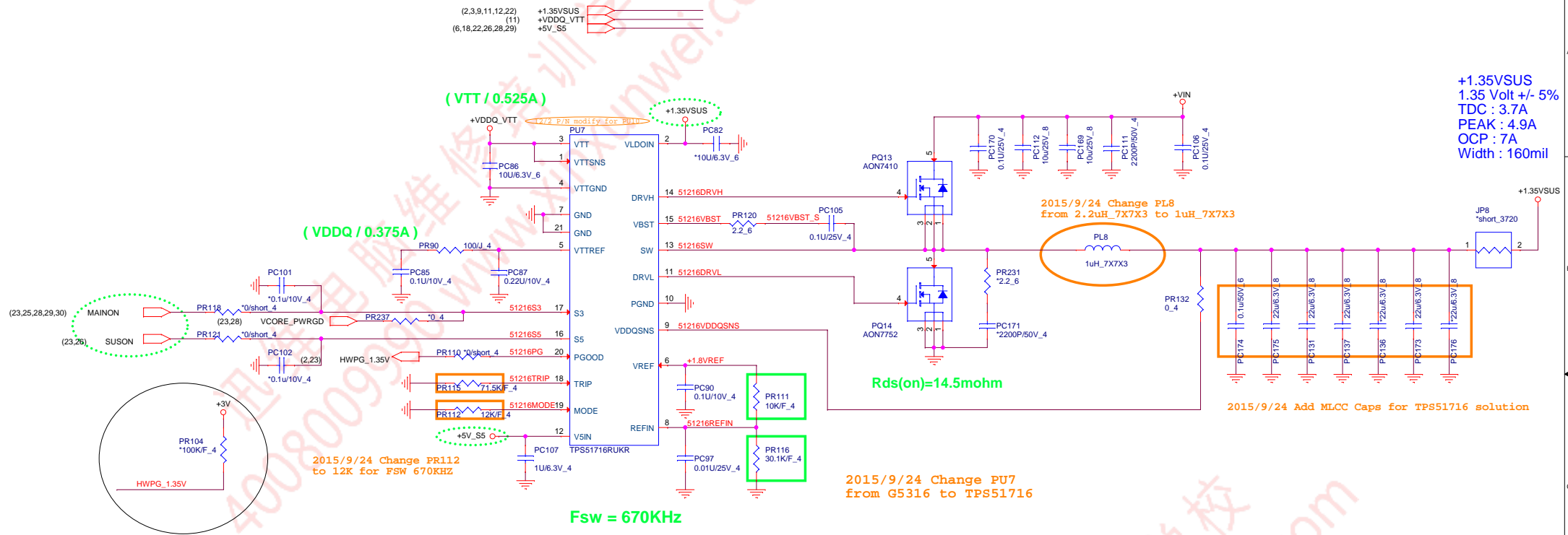
SPI NOR FLASH









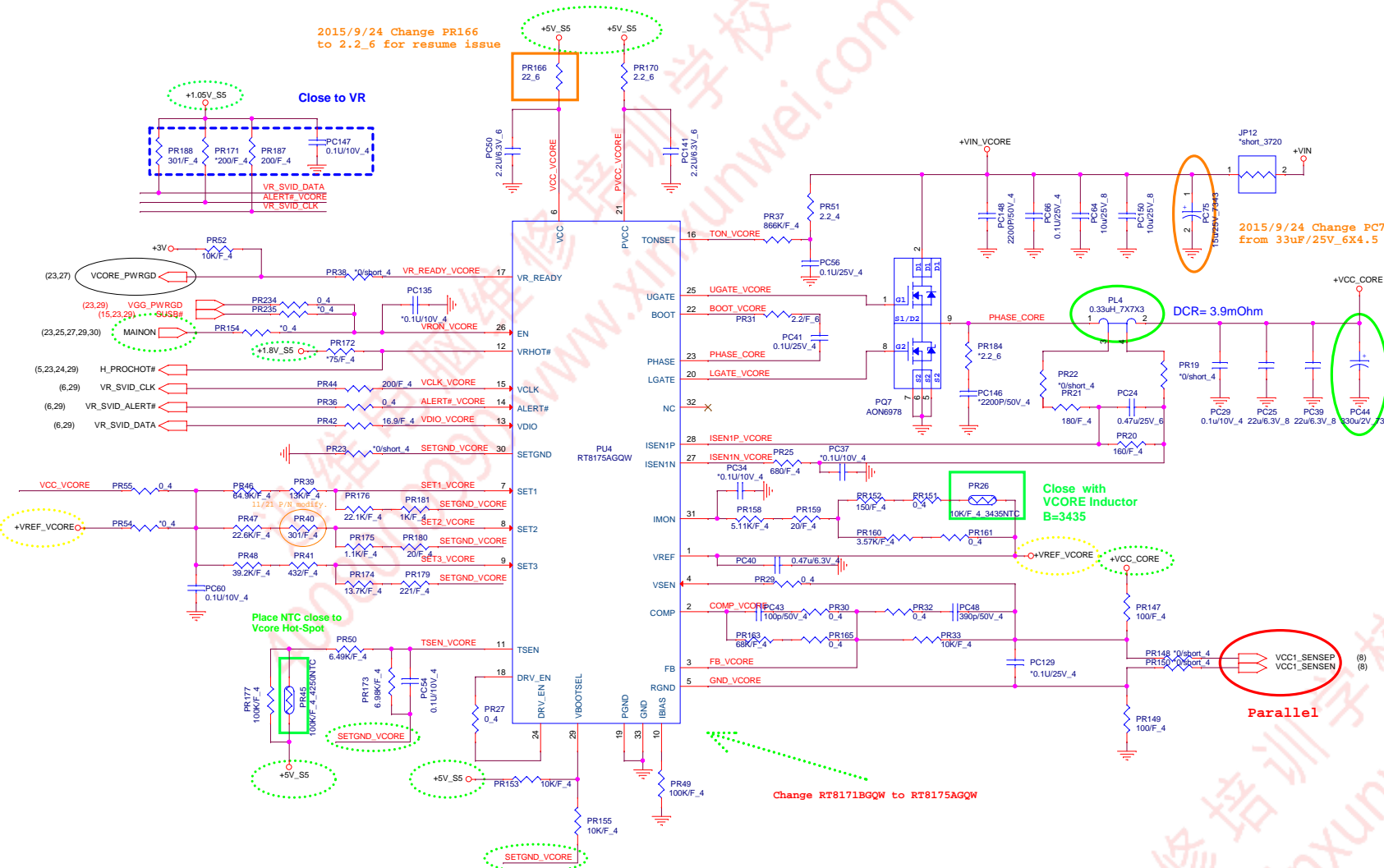


Mode	Frequency	Discharge mode
12K	670K	Tracking Discharge
1K	500K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

2015/9/24 Change PR166
to 2.2.6 for resume issue

Close to VR



VR 12.1

Braswell - VCC0+1 (1 Phase)

Icc TDC PL2 : TBD

Icc Max : 7A

OCP : 12.4A

Fsw : 800KHz

Vboot : 1V

VR address : 0

VCC0+1 L/L :

R_DC_LL : 0 mV/A

R_AC_LL : 0 mV/A



Quanta Computer Inc.

PROJECT : ZHW_ZHX

Size	Document Number	Rev
	VCC0+1 (RT8175)	1A
Date:	Friday, February 05, 2016	Sheet 28 of 31

2015/9/24 Change PR108
to 2.2_6 for resume issue

Close to VR

VR_READY_VGG

VR 12.1

Braswell - VGG (1 Phase)

Icc TDC PL2 : TBD

Icc Max : 15A

OCP : 20.7A

Fsw : 800KHz

VR Address : 5

VCORE L/L :

R_DC_LL : 0 mV/A

R_AC_LL : 0 mV/A


Parallel

Change RT8171BGQW to RT8175AGQW

Place NTC close to
Vcore Hot-Spot

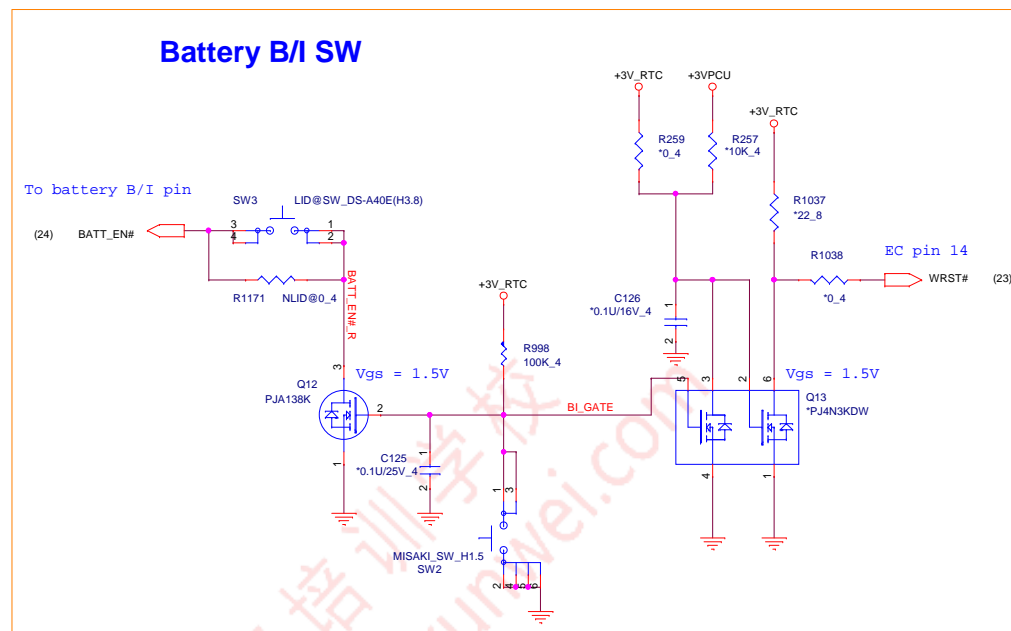
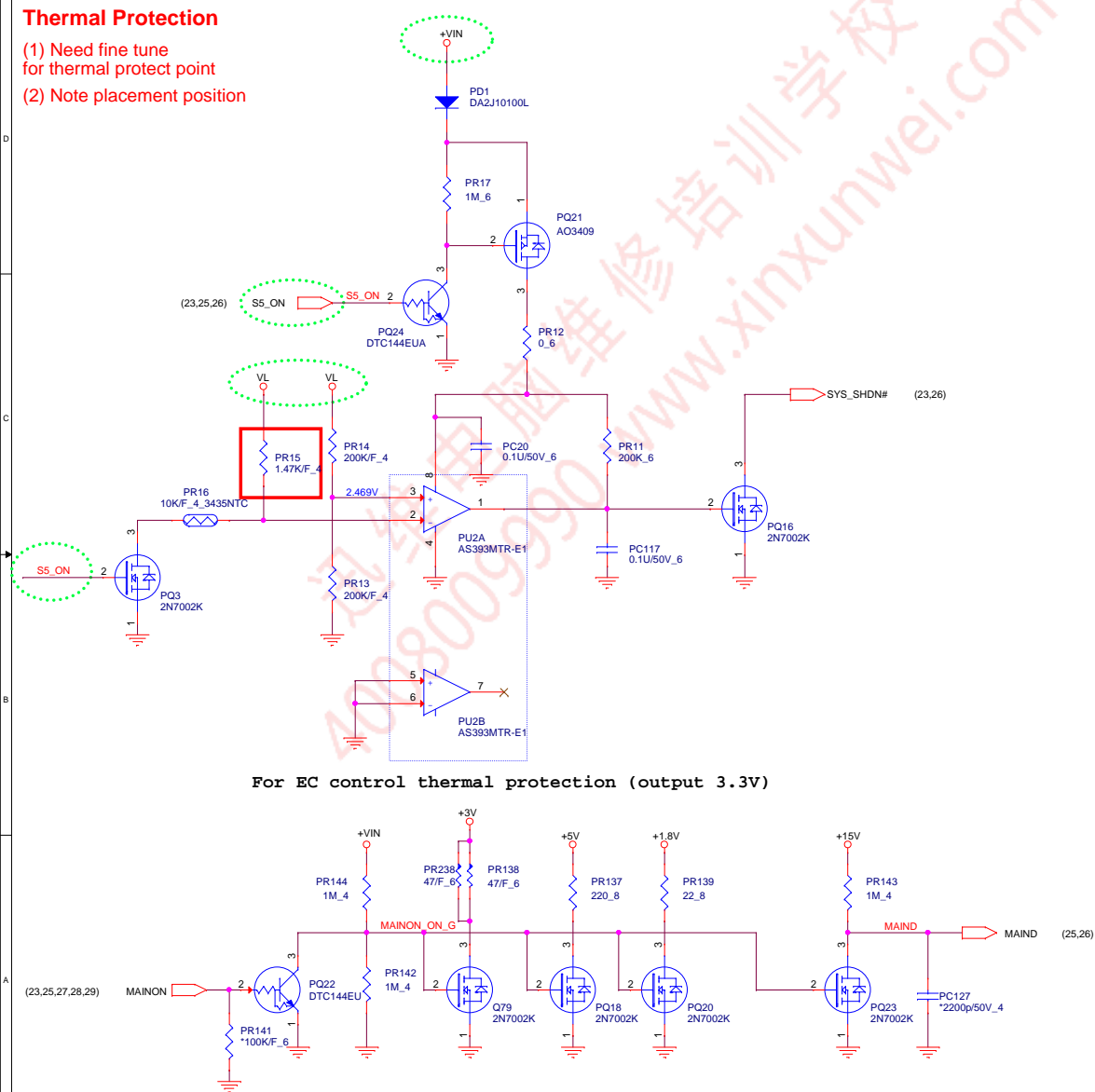
DCR= 3.9mOhm


Close with
VCORE Inductor
B=3435



 Quanta Computer Inc.			
PROJECT : ZHW_ZHX			
Size	Document Number	+VGG (RT8175)	
Date:	Friday, February 05, 2016	Sheet	29 of 31

Thermal Protection

- (1) Need fine tune for thermal protect point
(2) Note placement position



 Quanta Computer Inc. PROJECT : ZHW_ZHX			
Size	Document Number	Rev	
	Thermal / Discharge	1A	
Date:	Friday, February 05, 2016	Sheet	30 of 31

Model	Rev.	CHANGE LIST									
ZHKD	1A	2014/12/11 First Release									
<div>迅维电脑维修培训学校 4008009990 www.xinxunwei.com</div>											
DOC NO.	PROJECT MODEL :	ZHKD	APPROVED BY:		DATE:		<div> Quanta Computer Inc. PROJECT : ZHM_Z84</div>				
	PART NUMBER:		DRAWING BY:		REVISION:		<div> Change list</div>				